Analog Configurability-Test Scheme for an Embedded Op-Amp Module in TI MSP430 Microcontrollers

Agustín Laprovitta[1], Gabriela Peretti[2] and Eduardo Romero[2]

[1] Communication Lab, Facultad de Ingenieria, Universidad Católica de Córdoba, Av. Armada Argentina 3555, 5017 Córdoba, Argentina
alapro@uccor.edu.ar
[2] Mechatronics Research Group, Universidad Tecnológica Nacional Facultad Regional Villa María, Av. Universidad 450, 5900 Villa María, Argentina
gecam@frvm.utn.edu.ar

Abstract. This paper proposes the application of the analog configurability test (ACT) approach for an embedded analog configurable circuit, composed by operational amplifiers and interconnection resources that are embedded in the MSP430xG461x microcontrollers family, with the aim of verifying its mode programmability. This test strategy is particularly useful for applications involving in-field circuit reconfiguration, and require reliability and safe operation characteristics. The approach minimizes the cost in hardware overhead by employing only the hardware and software resources of the microcontroller. An embedded test routine sequentially programs selected module configurations, sets the test stimulus, acquires data from the internal ADC, and performs required calculations to determine the gain of the block. The test approach is experimentally evaluated using an embedded-system based real application board. Our experimental results show very good repeatability, with very low errors. These results show that the ACT proposed here is useful for testing the functionality of the EACC under test in a real application context by using a simple strategy at a very low cost.

Keywords: built-in self-test; mixed signal testing; embedded analog test; microcontroller test.

1 Introduction

The analog portion of system-on-chip (SoC) or mixed-signal integrated circuits (ICs) is usually relatively small compared to its digital counterparts. However, testing analog circuits poses a number of unique testing problems when compared to digital ones and, as result, a variety of different and unique tests architectures and approaches are required [3]. This particular situation characterizes the embedded analog and mixed-signal configurable sections included in modern microcontrollers (μCs).

Testing an embedded analog configurable circuit (EACC) in a μC is a significant challenge due to the lack of controllability / observability of its internal nodes and the usually high number of available configurations. The later causes that the direct test application and response evaluation is almost never possible [11]. On the other hand,

there are no widely accepted analog fault models, as is the case in digital testing. Consequently most analog testing schemes tend to be specification-oriented as opposed to defect-oriented approaches, typically used in digital circuits test.

Under the assumption that the processor core is fault free, the testing of analog or mixed-signal embedded cores can be done by the microprocessor, according with the method presented in [10]. A program (which is stored in an external memory) is developed to generate the necessary test stimuli. The response of the circuit under test (CUT) could be either evaluated concurrently by automatic tester equipment (ATE) or stored in the on-chip memory for later evaluation. Unfortunately, this approach is oriented to fixed-function embedded cores in production test.

In fact, a relatively low number of papers related to the test of analog configurable circuits have been reported. In [15] and [6], an online testing strategy for continuous-time field programmable analog arrays (FPAAs) is presented. In [1-2] and [9], well-known off-line techniques such as oscillation-based test (OBT) and transient analysis method (TRAM) have been successfully applied to FPAAs. However, the use of these strategies for in-field test applications is very limited because the addressed FPAA supports a limited number of configuration cycles, and the implementation of the test routine requires a high number of reconfiguration procedures.

A self-test strategy for an EACC, named as analog configurability test (ACT), is presented in [7]. The ACT strategy minimizes the cost in hardware overhead by employing only the hardware and software resources of the microcontroller, programming a reduced set of available configurations for the EACC and testing its functionality by measuring only a few key parameters. The processor executes an embedded test routine that sequentially programs different configurations, acquires data from an embedded ADC and performs required calculations.

In this paper, we demonstrate that the ACT approach can be extended to a different platform than the used in [7]. An EACC composed by operational amplifiers (OAs) and interconnection resources that is present in the MSP430x461x μCs family from Texas Instruments® is taken as a case study with the aim of verifying its mode configurability. It should be noted that the addressed EACC has different characteristics and functionalities than the adopted in [7], and consequently, the configurations set and the test procedures must be reformulated, as usual in analog test strategies, for this new circuit. In addition, the resources available on chip for testing purposes are quiet different, allowing some refinements in the test procedures.

The ACT experimental evaluation was performed in an embedded-system based application board, which consists in a wireless sensor network (WSN) node with a multi-sensor interface capability. This constitutes another important contribution of the present work since it is the first time that the performance of the ACT approach is evaluated in a real application context. The approach is oriented to be used as a low-cost self-test procedure for maintenance purposes, establishing the configurations that can be effectively programmed by the processor core, before a reconfiguration process. By other way, ACT could be part of a broader software-based built-in self-test (SW-BIST) strategy. In SW-BIST, a microprocessor core functions as pattern generator and response analyzer to test other components embedded in the system [4 - 5], [8].

2 Test Considerations

The μC adopted as case study (MSP430FG4619) is based on a 16-bits RISC CPU and includes several digital, analog and mixed-signal modules on-chip. The block diagram of the system, obtained from the datasheet provided by the vendor is depicted in Fig.1. This figure shows the CUT (OAMs) and highlighted the blocks used by the ACT proposed.

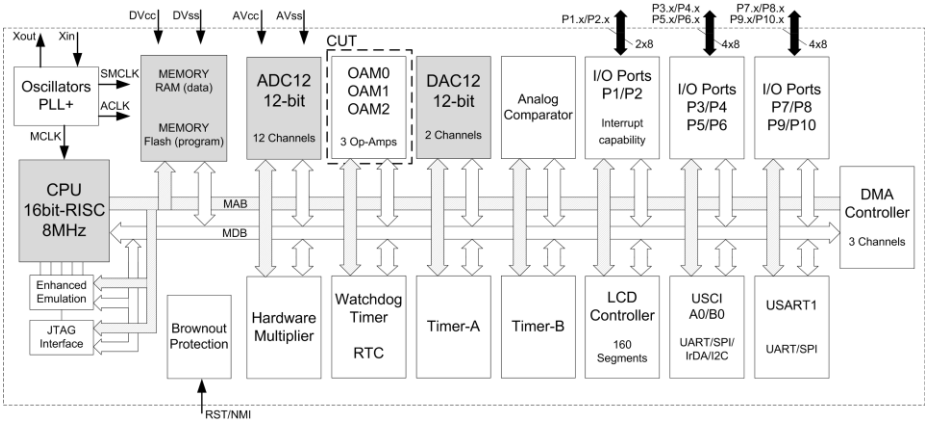

Fig. 1. Block diagram of the microcontroller chosen as a case study.

The EACCs are so-called OA modules (OAM) by the vendor, and three of them (OAM0, OAM1, and OAM2 in Fig. 1) are implemented in the device. The functional diagram of one of these modules is depicted in Fig. 2. As it is shown, an OA (OAx), several analog multiplexers, a resistor ladder and other resources compose each OAM. The block configuration is register-based and is programmed by the user at runtime.

The multiplexer driven by the signal *Mode Selection* establishes the different OAM configurations, called by the manufacturer as *Modes* (see Table 1). A programmable resistor ladder (driven by *Gain Selection* signal) sets the gain in amplifier modes or a reference voltage level in the comparator mode. The signals *Output-1*and *Output-2 Selection* allow the connection of the OA output with the ADC and/or with dedicated analog output pins respectively. The internal combination of two or more OAMs, in order to achieve more complex configurations, is possible by means of the signals *OAxOUT, OAxTAP* and *OAxR bottom*. A detailed description of the module is out of the scope of this work, and is provided by the vendor in [13].

By a simple comparison between complete diagrams of EACCs taken as CUT in this work and in [7], reported by the manufacturer in [13] and [12] respectively, it is possible to observe the significant differences in the available input, output and feedback signal paths. Consequently, there are also differences in their configuration registers. The number of OAMs present in this device also makes the test an even more challenging task mainly due to the increase of the possible interconnection paths between them.

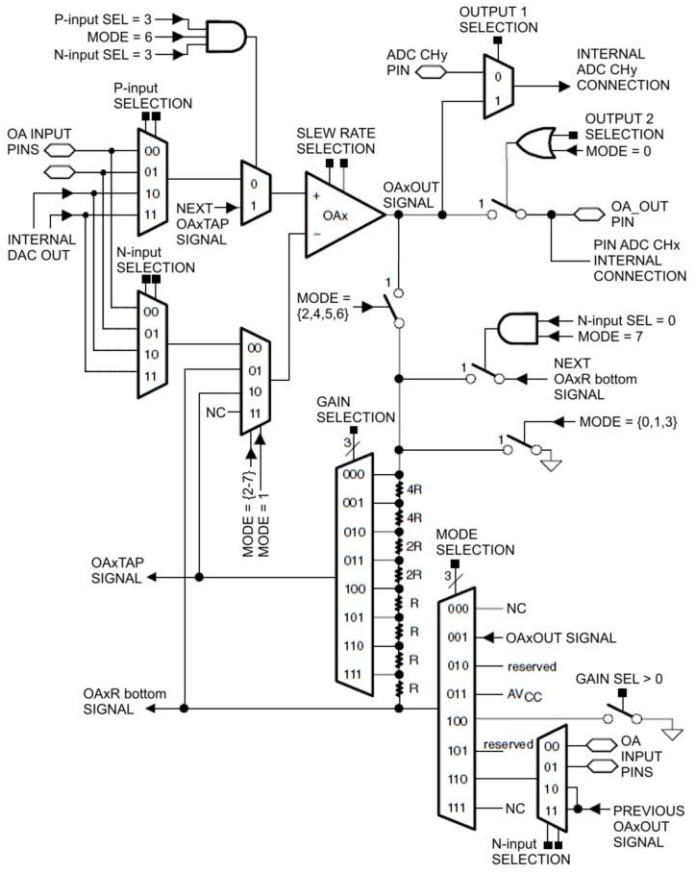

Fig. 2. Schematic diagram of the OA module.

Table 1. OAM modes.

Mode Selection signal value	OAM mode
0	General purpose OA
1	Unity gain buffer
2	Reserved
3	Comparator
4	Non-inverting PGA[1]
5	Reserved
6	Inverting PGA
7	Differential amplifier

[1] PGA: Programmable Gain Amplifier

It should be noted that, not all possible configurations of *N-input* and *P-input Selection* signals are evaluated in the test procedures. This is because the OA analog input pins are reserved for application purposes in normal operation. All the mode test procedures (with the only exception of mode 0) are performed using exclusively internal feedback paths.

For this case study, all the measurements in test mode are performed by using the internal ADC. As shown in Fig. 1, the module is a 12-bit SAR core converter with 12 input-channels (CH), sample select control and on-chip reference voltage generator. The analog supply voltage of the device (AV_{CC}) is set as the reference voltage for the ADC in order to be able to perform conversions in the entire OA operating range.

The ACT approach determines the correct configurability of each OAM mode by measuring the gain of the block in selected configurations. The on-chip digital to analog converter (DAC12 in Fig. 1) is used as test stimulus generator. Taking advantage of the availability of the DAC in this new platform, we propose two different voltage levels for each test (V_{IN1} and V_{IN2}) and calculate the gain in differential form in order to cancel the effect of the OA offset level:

$$G = (V_{OUT2} - V_{OUT1}) / (V_{IN2} - V_{IN1}) \quad (1)$$

Fixed gain values are used in the mode configurability test procedures. Consequently, not all the possible gains of the amplifier are exercised because it is assumed the right operation of the resistor ladder. The verification process of the resistor ladder is out of the scope of this work. Detailed information regarding this process can be found in [7].

3 Configurability Test Scheme

In order to test the complete OAM programmability, it is necessary to exercise all the combinations of the multiplexers, switches and configuration signals. In addition, all possible signal paths in the module should be used. For the circuit addressed in this paper, each OAM has a total of 15 configuration bits. If the *P-input Selection* (2bits) and *N-input Selection* (2bits) configuration signals are not taken into account because, as above-mentioned, we reserve the OA analog input pins for application purposes, the remaining signals produce 256 possible configurations for each value of *Mode Selection* (3bits) signal.

However, not all the combinations are valid for all the modes due to there are some programmed configurations that have no effect in the module operation. For example, if the module is programmed in mode 0 (General-purpose OA), the internal feedback loop is automatically disconnected and consequently, any change in the configuration signal *Gain Selection* does not produce changes in the signal path. Table 2 summarizes the number of valid combinations for each mode in the column labeled as "OAM valid configurations", based on the reduced structural information provided by the vendor in [13].

Table 2. OAM valid configurations

OAM mode	OAM valid configurations
Mode 0	12
Mode 1	24
Mode 3	192
Mode 4	192
Mode 6	384
Mode 7	192
Total	996

As can be inferred from this analysis, an exhaustive exercise of all the valid OAM configurations would be extremely costly in both time and power consumption. The ACT approach in [7] proposes, through a inspection process of the module schematic circuit, to determine the proper selection of test configurations that allows exercising all the possible states of the multiplexers and switches while covers all the signal paths for each module.

As it was mentioned in Section 1, the ACT proposed in this paper is aimed to determine only the correct configurability of the OAM modes reported in Table 1. To perform this task, the embedded test routine sequentially programs selected module configurations (to be discussed in the next sub-sections), sets the test stimulus, acquires data, and performs required calculations to determine the gain of the block. With these tests procedures, not all the states of multiplexers and switches are exercised. However, by implementing the test of additional characteristics like *Gain* and *Slew Rate Selection* functionalities (among others) it will be possible to achieve a complete coverage of the above mentioned states. These additional test procedures are out of the scope of this work and will be reported elsewhere. Space reasons preclude their inclusion in this paper.

3.1 Test of Modes 0 and 1

In both modes, the OAMs are configured as unity gain buffers for testing purposes. Mode 0 is designed to use the module with external components and all the internal feedback paths are isolated from the OAs. Consequently, for configuring the OA as unity gain buffer, we use the OA pins to connect the feedback loop. Fig. 3 shows the scheme adopted by the test routine. The feedback path is a wired connection that takes advantage of the existing components on the application circuit board. However, if the configuration in a different application did not include a resistor in the feedback path, the use of external analog multiplexers (to switch between test and normal operation) could be required. Otherwise, the test procedure for mode 0 can be overridden according with the test requirements of the application. In mode 1, the OA is configured as unity gain buffer using a dedicated internal feedback path.

The test procedure is the same for both modes. The OA output is connected to the ADC input channel assigned to the OAxOut pin (OA0, OA1 and OA2 with CH0, CH1 and CH2 respectively) by using the switch driven by *Output-2* and *Mode Selection* signals (see Fig. 2). The ADC also measures the OAM input signal (test

stimulus) from the DAC1 output through the CH7, assigned to the DAC1_Out pin. With these values, the on-chip processor computes the module gain.

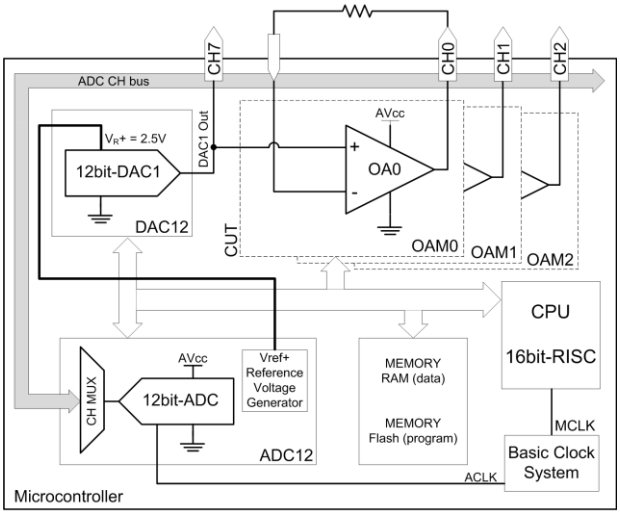

Fig. 3. Arrangement for testing mode 0

3.2 Test of Mode 3 - Comparator

In order to determine if each OAM can be configured as a comparator, we set a fixed voltage level at the non-inverter input of the OAs (V+) by using the DAC1 internal connection and program the inverter input with voltages obtained from the resistor ladder. By commuting the ladder between voltages higher and lower than V+, it is possible to verify if the comparator output transitions are within the values reported by the vendor in [14]. In this case, the ADC acquires the OA output values using the internal routing to the ADC CH12, CH13 and CH14 for OAM0, OAM1 and OAM2 respectively, by setting the signal *Output-1 Selection* (refer to Fig. 2).

3.3 Test of Mode 4 - Non-inverting PGA

In mode 4, each OAM is configured as a programmable-gain non-inverter amplifier. As shown in Fig. 4, DAC1 is used for exciting the OAMs, with DC voltage levels. For testing the mode programmability, the gain of each OAM is programmed in 2. We do not test all the possible gains of the amplifier because, as explained above, the right operation of the resistor ladder is out of the scope this work. The OAMs input stimulus level is registered through the ADC CH7, while the OAs outputs are measured as in the previous case (test of mode 3).

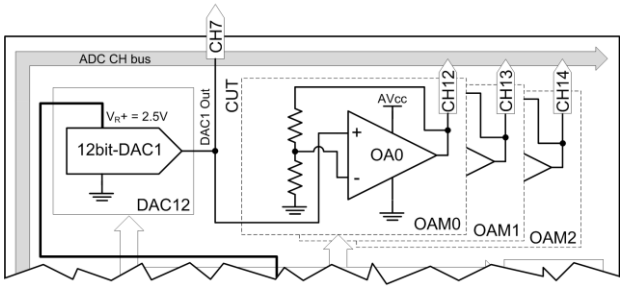

Fig. 4. Arrangement for testing mode 4

3.4 Test of Mode 6 - Inverting PGA

When an OAM in configured in mode 6 (programmable-gain inverting amplifier), the use of a DC voltage level as test stimulus from the DAC is not useful because the µC employs a single supply. As a consequence, a negative output swing is not possible. However, for testing mode 6 it is possible to configure the OAM as inverter amplifier but connect internally its input to ground by means of the proper configuration of the OA input pin. This can be observed in Fig. 5 for the module labeled as "CUT I".

Under the above-mentioned condition, if the OA non-inverter input is connected to a DC voltage from the DAC1, then the system behaves like a non-inverter amplifier with the CUT programmed in mode 6. In this way, it is possible to test individually the mode configurability of each OAM. As in the previous case, the gain of the amplifier is set in 2 and the ADC acquires the input /output levels of each module by means of the channels reported in Fig. 5.

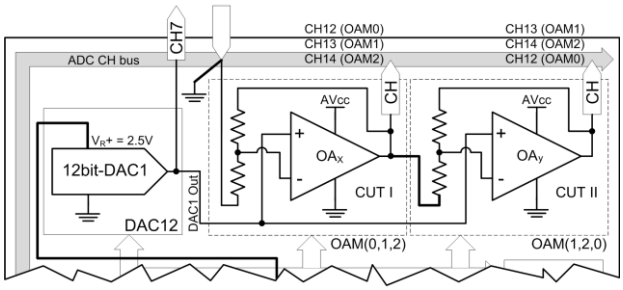

Fig. 5. Arrangement for testing mode 6

Another feature that characterizes an OAM in mode 6 is that it can be cascaded with the previous OAM output. This situation can be observed for the module labeled as "CUT II" in the Fig. 5. Since this feature implies a new signal interconnection path between blocks, the test routine also configures the pair of OAMs as shown in the

above-mentioned figure and registers the voltage level at the positive input of both OAs (V_{DAC1_Out}) and the output of the cascade connection (output of CUT II), named as $Vout_{OAy}$. In this way, the routine establishes if the cascade connection can be programmed, computing the gain achieved by the array. This process is repeated three times, one for each possible combination (OA0-OA1, OA1-OA2 and OA2-OA0).

Under these conditions, the gain of the cascaded amplifiers is:

$$G_{cascade} = Vout_{OAy} / V_{DAC1\_Out} = G_{OAx} \,.\, G_{OAy} + 1 - G_{OAy} \quad (2)$$

In (1), G_{OAx} and G_{OAy} are the programmed gain values for OAM_X and OAM_Y respectively. If this gain is not achieved for a given cascade connection, the interconnection path is declared faulty since each module has been previously tested individually.

3.5 Test of Mode 7 – Differential Amplifier

The µC adopted as a case study supports a three-OA differential-amplifier configuration. The manufacturer reports in [13] the OAMs setup for this configuration, depicted in Fig. 6. The output voltage is calculated as:

$$V_{diff} = (V_2 - V_1) \,.\, (R_2 / R_1) \quad (3)$$

For testing the mode configurability (mode 7), we inject a DC stimulus to the input labeled as V_2 by means of the DAC1, and V_1 is connected internally to power ground. Then, we evaluate through the ADC the OA_Z output (V_{diff}) and establish the gain value V_{diff} / V_2. This process is repeated three times, changing the OAM programmed on mode 7 (CUT).

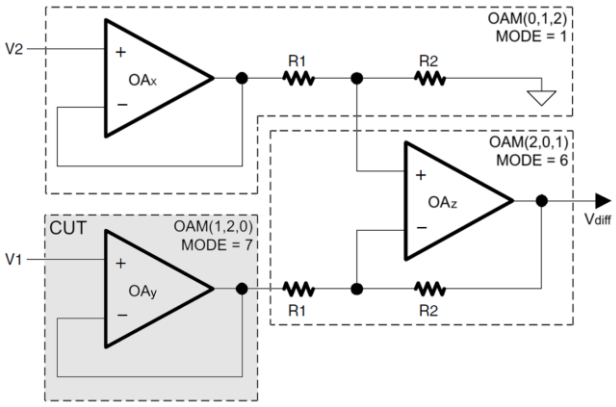

Fig. 6. Three-OA differential amplifier configuration

4 Experimental Results

As mentioned in Section 1, the ACT experimental evaluation was performed in a real application board, which consists in a WSN node developed from the concept of the abstraction layer sensor interface (see Fig. 7). Multiple sensors with both analog and digital interfaces can be used according to the applications requirements. The node uses the re-configuration capability of the analog and mixed signal resources in the μC to allow the direct connection of a wide range of sensors with different analog interfaces in a fixed hardware structure.

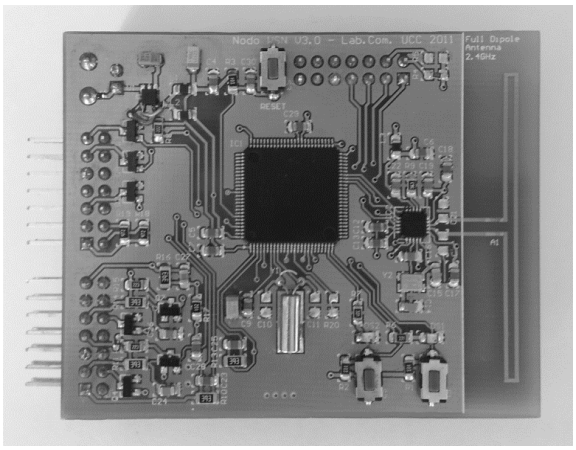

Fig. 7. WSN node application board

The embedded test routine has been written in C language as a library using IAR Embedded Workbench for TI MSP430 C/C++ compiler, and amounts to about 2Kbyte of program memory in the μC. The measurement repeatability at free air temperature is evaluated in order to assessing the test precision. For doing this task, the test procedure is repeated 100 times in each test condition.

The ADC inaccuracies (including offset, gain, and nonlinearity errors) introduce errors in the gain measurements performed by the routine. The total unadjusted error determines the overall deviation in the digital code delivered by the ADC from an ideal conversion. The datasheet reports a typical value of ±2LSB for this parameter with a maximum of ±5LSB, what it means a maximum deviation of ±3.052mV for our test conditions. This value is considered here as the limiting error of the voltage measurements, neglecting the noise.

The experimental results for modes 0, 1, 4, 6 and 7 are reported in Table 3. The column labeled as "Parameter" shows the specific gains evaluated by the test routine for each OAM mode. The column labeled as "Test setup" shows the expected value for these parameters and gives the value of the *Gain Selection* signal (see Fig. 2). The mean values shown in the table are a measure of central tendency, while the maximum (Max) and the minimum (Min) values are a measure of dispersion.

Table 3. Experimental test results.

Test mode	Parameter	Test setup	Min	Mean	Max
Mode 0	Unity gain OAM0		0.9939	1.0013	1.0075
	Unity gain OAM1		0.9917	1.0010	1.0083
	Unity gain OAM2		0.9947	1.0011	1.0114
Mode 1	Unity gain OAM0		0.9969	1.0026	1.0091
	Unity gain OAM1		0.9954	1.0025	1.0098
	Unity gain OAM2		0.9916	0.9979	1.0045
Mode 4	Gain OAM0	Programmed gain = +2 Gain selection = 2	1.9879	2.0036	2.0167
	Gain OAM1		1.9924	2.0041	2.0182
	Gain OAM2		1.9894	2.0025	2.0152
Mode 6	Gain OAM0	Programmed gain = +2 Gain selection = 2	1.9894	2.0020	2.0198
	Gain OAM1		1.9894	2.0029	2.0167
	Gain OAM2		1.9939	2.0035	2.0167
	Gain OAM2–OAM0 in cascade	Programmed gain = 0.665 Gain selection OAM2 = 1 Gain selection OAM0 = 2	0,6626	0,6672	0,6727
	Gain OAM0–OAM1 in cascade	Programmed gain = 0.665 Gain selection OAM0 = 1 Gain selection OAM1 = 2	0,6619	0,6668	0,6717
	Gain OAM1–OAM2 in cascade	Programmed gain = 0.665 Gain selection OAM1 = 1 Gain selection OAM2 = 2	0,6611	0,6672	0,6709
Mode 7	Gain of arrangement OAM0-OAM1-OAM2	Programmed gain = 1.666 CUT = OAM1	1,6591	1,6724	1,6823
	Gain of arrangement OAM1-OAM2-OAM0	Programmed gain = 1.666 CUT = OAM2	1,6591	1,6721	1,6818
	Gain of arrangement OAM2-OAM0-OAM1	Programmed gain = 1.666 CUT = OAM0	1,6601	1,6730	1,6859

The data shows that the measurement repeatability is very good for all the modes tested. The highest observed deviation is 1.02% in mode 0. By other way, the mean values are very close to the expected for each programmed configuration, with a maximum deviation of 0.38% in mode 7.

The test of mode 3 shows that all the OAMs, configured as comparators, give output excursions between 3.3mV and values near AV_{CC}, for the 100 repeated test executions. This range agrees with the data reported by the vendor in the datasheet [14].

5 Conclusions

In this paper, we described the application of the ACT approach to an EACC composed by operational amplifiers and interconnection resources of a modern µC, in order to verify its mode configurability. The test procedures were successfully adapted to the requirements of the new circuit. The negligible hardware overhead of the test scheme allows using it in applications that require minimizing power or cost. Additionally, due to the modularity of the scheme, some steps involved in the test can

be avoided for reducing even more power and test time. The test strategy is experimentally evaluated in a WSN node with multi-sensor interface capability in order to demonstrate the ACT approach applicability in the context of a real application. The experimental results show very good repeatability, with very low errors. These results allow concluding that the approach proposed here is useful for testing the functionality of the CUT using a simple and very low cost strategy.

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